



Hardware Based Flash Memory Failure Characterization Platform

Greg Bray
B.S. Computer Engineering
University of Utah

<http://code.google.com/p/2007-uofu-micron-clinic/>



Background:

- Graduated in May 2008 with B.S. Computer Engineering
- Capstone experience: ECE Engineering Clinic Program
 - “*Students working with industry on real-world projects*”
Program director Steve Blair - <http://www.ece.utah.edu/clinics>
 - Teams consists of 4-6 Senior EE or CE students
 - Each team has Faculty advisor and Industry liaisons
 - Sponsor company defines scope of the problem
 - Students propose solution and design system over 2 semesters
 - Culminates in ECE open house presentation and IEEE paper
- Provides a great opportunity for students to work with industry leaders (Micron, L-3 Communications, Rocky Mountain Power, GE Healthcare, Motorola...)

Acknowledgements:

- 2007-2008 ECE Engineering Clinic teammates
 - Greg Bray (Team Lead, CE)
 - Kyle Stewart (Technical Lead, CE)
 - Jeffrey Gorton (Documentation Lead, EE)
 - Jonathan Morgan (Data Analyst, EE)
 - Garrett Thomas (Quality Assurance, EE)
- Faculty Advisor – Ken Stevens
- Clinic Sponsor – Micron Foundation
 - Assistance from Dennis Zattiero and Dean Klein

Section Outline:

- Introduction: background, project goals, and intended use
- Hardware Platform for Flash Failure Characterization
 - Altera DE2 FPGA using modular System-On-A-Programmable-Chip (SOPC) architecture
 - Flash daughter card interface for FPGA
 - Verilog based NAND controller quickly executes commands on Flash device and returns results to C based firmware for processing.
 - Interactive C# based GUI on host PC for creating Flash test scripts, collecting failure results in MS SQL database, and analyzing failure data.
- Live project demonstration and results

More information (documentation, executables, source code, etc):

<http://code.google.com/p/2007-uofu-micron-clinic/>

Introduction: Background

- NAND Flash is increasingly being used in consumer devices
 - low cost, low power, shock resistant and non-volatile!
- Memory blocks wear out after extended use
 - Manufacture guarantees 100,000 program/erase cycles
- Very little is know as to the failure characteristics after 100,000
 - Varies between vendors, models and production runs
- Techniques can be used to extend lifetime, but which to use?
 - Need a way to find failure characteristics

Introduction: Project Goals

- Low cost and simple platform for testing NAND flash memory
- Allow product engineers to test using their own test scripts
- Provide tools for analyzing failure rates (reports, graphs, images)
- Provide preliminary research regarding failure rates beyond manufactures stated limits
- Release the software and hardware designs under an open source license so that others can use the test platform and expand the features and functionality.

Introduction: Intended Use

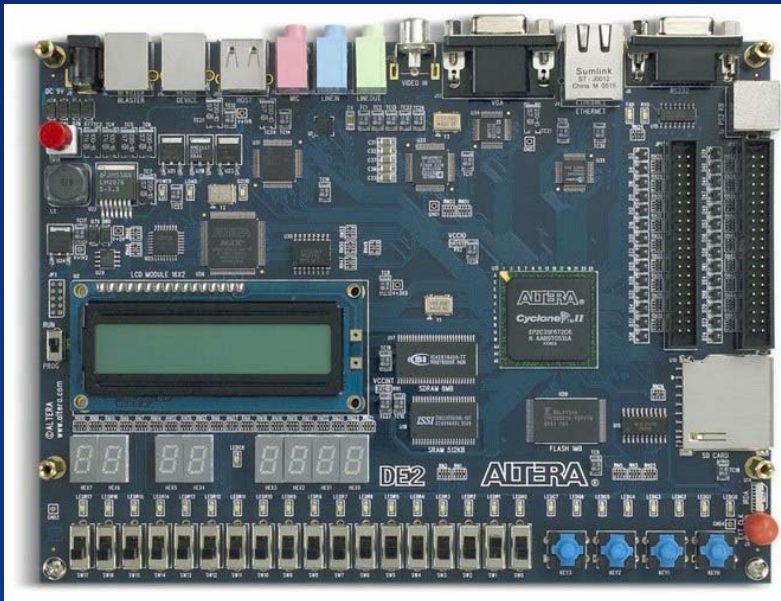
- Academic: Increase research on NAND Flash failure rates
 - How long before a chip contains 50% bad blocks or 95% bad blocks?
 - Are some blocks more likely to fail than others? Are there any patterns?
 - How severe are the failures? Small bit failures can be corrected using ECC.

- Product Design: Allow engineers to create better products
 - Given a specific use pattern and failure rate, what techniques should be used to optimize product lifetime? (Error Correction Codes, Bad Block Management, Graceful Device Deterioration)

- Industry: Allow for comparison of different Flash vendors and technologies by running the same test scripts on multiple chips

Hardware: Altera DE2 FPGA

- Altera DE2 Development Board:
 - Field-Programmable Gate Array (FPGA)
 - NIOS II Soft Processor
 - On-Chip Memory
 - USB
 - LCD Display and LEDs
- 48 pin TSOP Socket Daughter Card:
 - 40 pin IDE cable connection
 - 8 test pins on board
 - Supports 3.3v and 1.8v
 - Spring loaded socket for easy swapping
 - Produced by Boise State University



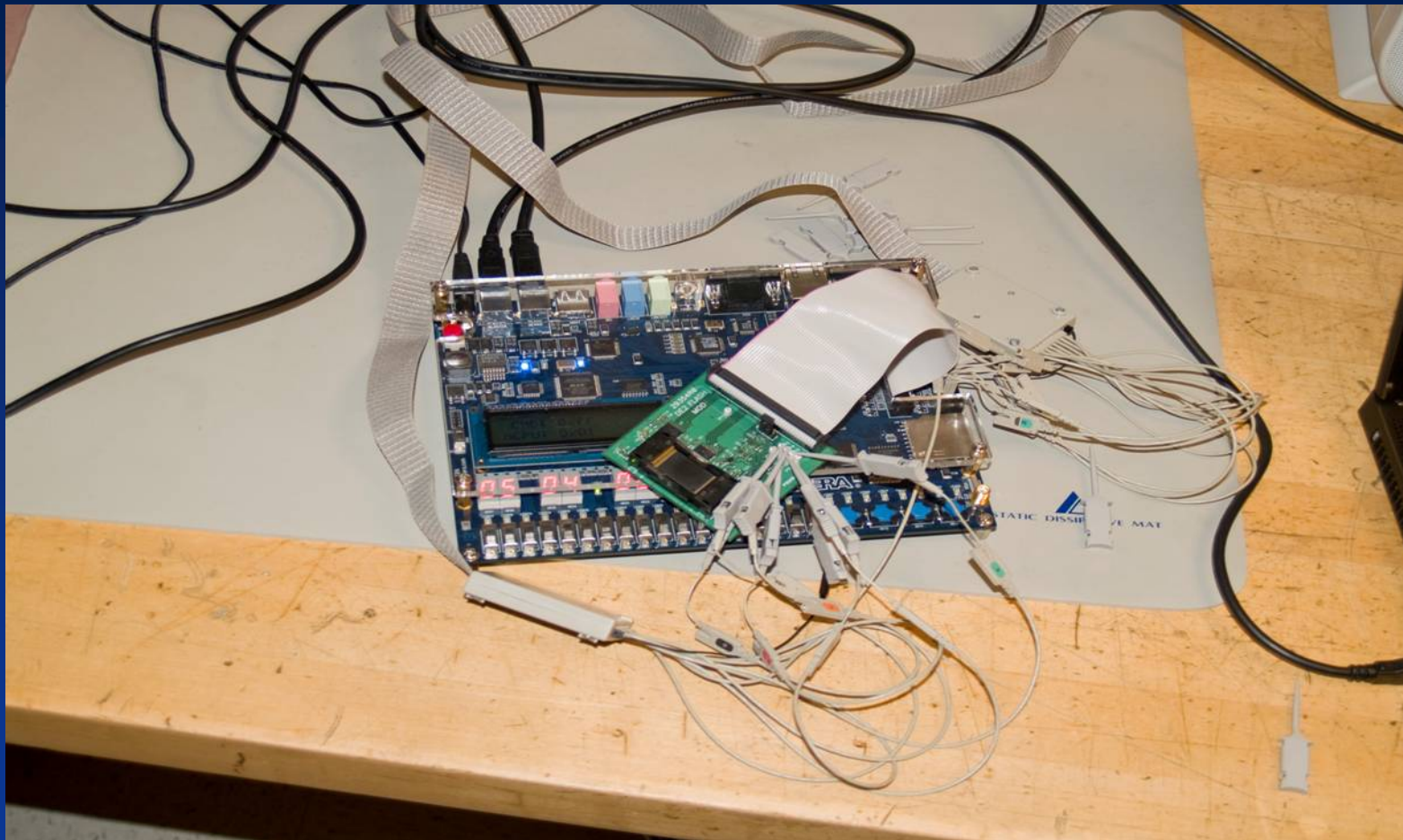
Software: Firmware, GUI, MS SQL

- FPGA runs Verilog based System On A Chip (SOPC)
 - Includes CPU, RAM, USB controller, Custom Flash Controller, etc...
 - Modular system. Can add or remove components very easily
 - Use Altera Quartus II software to customize hardware (free license)

- Firmware is written in C using NIOS II IDE (free license)
 - Communicates with host computer using USB interface
 - Queues up commands from host and issues them to custom NAND Flash controller for execution on Device Under Testing (DUT)
 - Collects results from DUT and sends data to host computer

- Graphical User Interface (GUI) written in C#
 - Allows user to define, load and save command scripts
 - Sends commands to FPGA and stores results in MS SQL database
 - Provides tools for analyzing flash failure data (reports, images, etc)

Live Demonstration

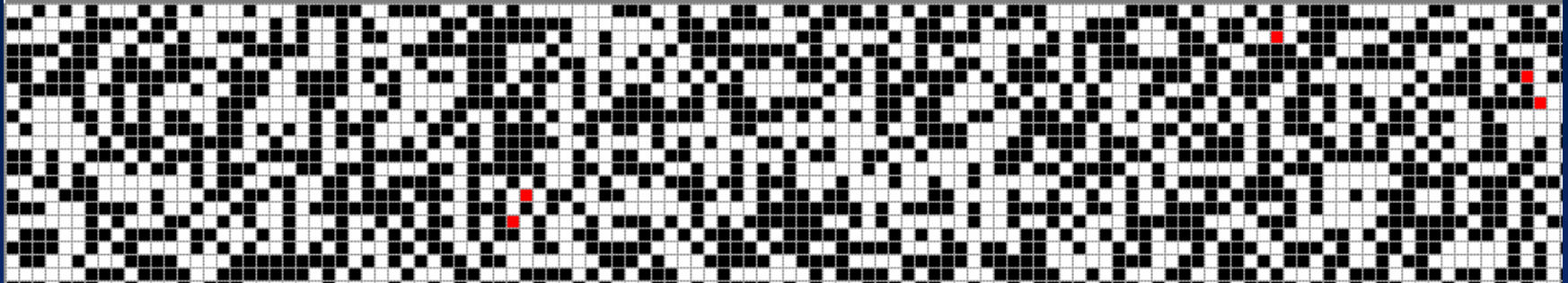


March 2008 – NAND Flash project with digital probes connected for troubleshooting

Results: Incomplete

- Project is still in Beta stage
 - Feature complete but not always stable
 - Platform is strong and well built, just needs to go through more iterations of testing and debugging
- Original project team has dissolved
 - All team members have graduated and moved on to other ventures (full time job, grad school, etc)
 - Work may continue under another clinic team this fall or other industry/academic groups
- Testing can take a long time
 - 100,000 cycles on a 4gb chip can take 3+ months!!!

Results: Simulated Image Analysis



Error Correction Level	Bits Required in the NAND Flash Spare Area		
	Hamming	Reed-Solomon	BCH
1	13	18	13
2	N/A	36	26
3	N/A	54	39
4	N/A	72	52
5	N/A	90	65
6	N/A	108	78
7	N/A	126	91
8	N/A	144	104
9	N/A	162	117
10	N/A	180	130

- Bit
- Tir

Future Work:

- Expansion of compatible chips
 - Currently only works with Micron 8x 48-Pin TSOP SLC NAND Flash
 - SOPC framework allows drop in replacement of our NAND controller with a new Verilog controller for another vendor or memory type.

- Ability to test multiple chips simultaneously
 - Altera DE2 Board has 2 IDE channels, currently one is used for connecting to DUT and the other is for troubleshooting with digital probe
 - Could add a second instance of the NAND Controller module to support testing multiple chips at the same time.

- Research the failure characteristics of flash memory
 - Can take 3 months or more to run 100,000 program/erase cycles on the entire address space.

More Information:

- Project website: <http://code.google.com/p/2007-uofu-micron-clinic/>
 - Source code, documentation, setup guide, research papers
- Altera website: <http://www.altera.com>
 - DE2 development board (\$269 academic, \$495 commercial)
 - Quartus II 8.0 Web Edition (free license for non-commercial use)
 - Nios II 8.0 Web Edition (free license for non-commercial use)
- Visual Studio Express website: <http://www.microsoft.com/express/2005/>
 - Visual C# 2005 Express Edition (free license)
 - SQL Server 2005 Express Edition (free license)